16Gb DDR5 SDRAM Addendum

MT60B4G4, MT60B2G8, MT60B1G16
Die Revision D

Features

This document describes the product specifications that are unique to Micron 16Gb DDR5 Die Revision D device. For general Micron DDR5 SDRAM specifications, see the Micron DDR5 SDRAM Core Product Data Sheet. Content in this 16Gb Die Revision D DDR5 SDRAM data sheet addendum supersedes content defined in the core data sheet.

- V_{DD} = V_{DDQ} = 1.1V (NOM)
- V_{PP}= 1.8V (NOM)
- On-die, internal, adjustable V_{REF} generation for DQ, CA, CS
- 1.1V pseudo open-drain I/O
- TC maximum up to 95°C
  - 32ms, 8192-cycle refresh up to 85°C
  - 16ms, 8192-cycle refresh at >85°C to 95°C
- 32 internal banks (x4, x8): 8 groups of 4 banks each
- 16 internal banks (x16): 4 groups of 4 banks each
- 16n-bit prefetch architecture
- 1 cycle/2 cycle command structure
- 2N mode
- All bank and same bank refresh
- Multi-purpose command (MPC)
- CS/CA training mode
- On-die ECC (bounded fault)
- ECC transparency and error scrub
- Decision feedback equalization (DFE)
- Loopback mode
- Command-based non-target (NT) nominal, DQ/DQS park, and dynamic WR on-die termination (ODT)
- sPPR and hPPR capability
- MBIST/mPPR capability
- Per-DRAM addressability
- JEDEC JESD-79.5 compliant

Options[1]	Marking
• **Configuration**	
– 4 Gig x 4	4G4
– 2 Gig x 8	2G8
– 1 Gig x 16	1G16
• **FBGA SDP Packages** (Pb-free)	
– x4, x8 78-ball (7.5mm x 11mm)	RZ
– x16 102-ball (7.5mm x 14mm)	HD
• **Timing** – cycle time	
– 0.357ns @ CL = 46	-56B
– 0.312ns @ CL = 52	-64B
– 0.277ns @ CL = 58	-72B
• **Operating temperature**	
– Commercial (0°C < T_C < 95°C)	None
– Industrial (-40°C < T_C < 95°C)	IT
• Die Revision	:D

Notes: 1. Not all options listed can be combined to define an offered product. Use the part catalog search on micron.com for available offerings.

Table 1: 16Gb Addressing

Configuration		4Gb x4	2Gb x8	1Gb x16
Bank address	Number of bank groups/number of banks per bank group/number of banks	8 / 4 / 32	8 / 4 / 32	4 / 4 / 16
	Bank group address	BG0-BG2	BG0-BG2	BG0-BG1
	Bank address in a bank group	BA0-BA1	BA0-BA1	BA0-BA1
Row address		R0-R15[1]	R0-R15[1]	R0-R15
Column address		C0-C10	C0-C9	C0-C9
Page size		1KB	1KB	2KB
Chip IDs/maximum stack height		CID0-3 / 16H	CID0-3 / 16H	CID0-3 / 16H

Table 2: Part Numbers and Timing Parameters

Part Number	Configuration	Memory Clock/ Data Rate	Clock Cycles ($CL\text{-}_nRCD\text{-}_nRP$)	^tAA (ns)	^tRCD (ns)	^tRP (ns)	Designation[1]
MT60B4G4RZ-56B:D	4Gb x4	0.357ns/ 5600 MT/s	46-45-45	16.000	16.000	16.000	Production
MT60B2G8RZ-56B:D	2Gb x8	0.357ns/ 5600 MT/s	46-45-45	16.000	16.000	16.000	Production
MT60B2G8RZ-56B IT:D	2Gb x8	0.357ns/ 5600 MT/s	46-45-45	16.000	16.000	16.000	Production
MT60B1G16HD-56B:D	1Gb x16	0.357ns/ 5600 MT/s	46-45-45	16.000	16.000	16.000	Production
MT60B1G16HD-56B IT:D	1Gb x16	0.357ns/ 5600 MT/s	46-45-45	16.000	16.000	16.000	Production
MT60B4G4RZ-64B:D	4Gb x4	0.312ns/ 6400 MT/s	52-52-52	16.000	16.000	16.000	Production
MT60B2G8RZ-64B:D	2Gb x8	0.312ns/ 6400 MT/s	52-52-52	16.000	16.000	16.000	Production
MT60B2G8RZ-64B IT:D	2Gb x8	0.312ns/ 6400 MT/s	52-52-52	16.000	16.000	16.000	Production
MT60B1G16HD-64B:D	1Gb x16	0.312ns/ 6400 MT/s	52-52-52	16.000	16.000	16.000	Production
MT60B1G16HD-64B IT:D	1Gb x16	0.312ns/ 6400 MT/s	52-52-52	16.000	16.000	16.000	Production
MT60B4G4RZ-72B:D	4Gb x4	0.277ns/ 7200 MT/s	58-58-58	16.000	16.000	16.000	Advance
MT60B2G8RZ-72B:D	2Gb x8	0.277ns/ 7200 MT/s	58-58-58	16.000	16.000	16.000	Advance
MT60B1G16HD-72B:D	1Gb x16	0.277ns/ 7200 MT/s	58-58-58	16.000	16.000	16.000	Advance

Notes: 1. **Production**: Although considered final, these specifications are subject to change as further product development and data characterization sometimes occur. **Preliminary**: For evaluation and reference purposes only and are subject to change by Micron without notice. Products are only warranted by Micron to meet Micron's production data sheet specifications. **Advance**: Contains initial descriptions of products still under development. For evaluation and reference purposes only and are subject to change by Micron without notice. Products are only warranted by Micron to meet Micron's production data sheet specifications.

Figure 1: Order Part Number Example

Example Part Number: MT60B2G8RZ-64B:D

Configuration	
4 Gig x 4	4G4
2 Gig x 8	2G8
1 Gig x 16	1G16

Package	Mark
78-ball 7.5mm x 11.0mm FBGA	RZ
102-ball 7.5mm x 14.0mm FBGA	HD

Revision
:D

Case Temperature	
Commercial	None
Industrial temperature	IT

Speed Bin	Cycle Time, CAS Latency
-56B	^{t}CK = 0.357ns, CL = 46
-64B	^{t}CK = 0.312ns, CL = 52
-72B	^{t}CK = 0.277ns, CL = 58

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General Notes and Functional Block Diagrams

General Notes

- The functionality and the timing specifications discussed in this data sheet are for the DLL enable mode of operation (normal operation), unless specifically stated otherwise.
- Throughout the data sheet, the various figures and text refer to DQs as "DQ." The DQ term is to be interpreted as any and all DQ collectively, unless specifically stated otherwise.
- The terms "_t" and "_c" are used to represent the true and complement of a differential signal pair. These terms replace the previously used notation of "#" and/or over-bar characters. For example, differential data strobe pair DQS, DQS# is now referred to as DQS_t, DQS_c.
- The term "_n" is used to represent a signal that is active LOW and replaces the previously used "#" and/or overbar characters. For example: CS# is now referred to as CS_n.
- The terms "DQS" and "CK" found throughout the data sheet are to be interpreted as DQS_t, DQS_c and CK_t, CK_c respectively, unless specifically stated otherwise.
- Complete functionality may be described throughout the entire document; any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.
- Any specific requirement takes precedence over a general statement.
- Any functionality not specifically stated here within is considered undefined, illegal, and not supported, and can result in unknown operation.
- Addressing is denoted as BG[*n*] for bank group, BA[*n*] for bank address, and A[*n*] for row/col address.
- A NOP is considered a valid command for very specific states such as power-down exit, self-refresh exit, and reset. The NOP must satisfy any associated command timings with respect to the preceding valid command.
- Not all features described within this document may be available on the Rev. A (first) version.
- Not all specifications listed are finalized industry standards; best conservative estimates have been provided when an industry standard has not been finalized.
- Although it is implied throughout the specification, the DRAM must be used after reaching a stable power-on level, which is achieved by following the proper voltage ramp and power-up initialization sequence procedures as outline in this specification.
- Not all features designated in the data sheet may be supported by earlier die revisions due to late definition by JEDEC.

Definitions of the Device-Pin Signal Level

- HIGH: A device pin is driving the logic 1 state.
- LOW: A device pin is driving the logic 0 state.
- High-Z or (HI-Z/Hi-Z): A device pin is tri-state
- ODT: A device pin terminates with the ODT settings, which could be terminating or tri-state depending on the mode register settings.

Definitions of the Bus Signal Level

- HIGH: One device on the bus is HIGH, and all other devices on the bus are either ODT or High-Z. The voltage level on the bus is nominally V_{DDQ}.
- LOW: One device on the bus is LOW, and all other devices on the bus are either ODT or High-Z. The voltage level on the bus is nominally $V_{OL(DC)}$ if ODT was enabled, or V_{SSQ} if High-Z.
- High-Z or (HI-Z/Hi-Z): All devices on the bus are High-Z. The voltage level on the bus is undefined as the bus is floating.

- ODT: At least one device on the bus is ODT, and all others are High-Z. The voltage level on the bus is nominally V_{DDQ}.
- The specification requires 8,192 refresh commands within 32ms between 0°C and 85°C. This allows for a ^{t}REFI of 3.9µs in normal refresh mode. The specification also requires 8,192 refresh commands within 16ms between 85°C and 95°C. This allows for a ^{t}REFI of 1.95µs in normal refresh mode.

Industrial Temperature

An industrial temperature (IT) device option requires that the case temperature not exceed below –40°C or above 95°C. JEDEC specifications require the refresh rate to double when T_C exceeds 85°C; this also requires use of the high-temperature self-refresh option. Additionally, ODT resistance and the input/output impedance must be derated when operating outside of the commercial temperature range, when T_C is between
–40°C and 0°C.

Automotive Temperature

The automotive temperature (AT) device option requires that the case temperature not exceed below –40°C or above 105°C. The specifications require the refresh rate to 2X when T_C exceeds 85°C; 4X when T_C exceeds 95°C. Additionally, ODT resistance and the input/output impedance must be derated when operating temperature Tc <0°C.

Figure 2: 4 Gig x4 Functional Block Diagram

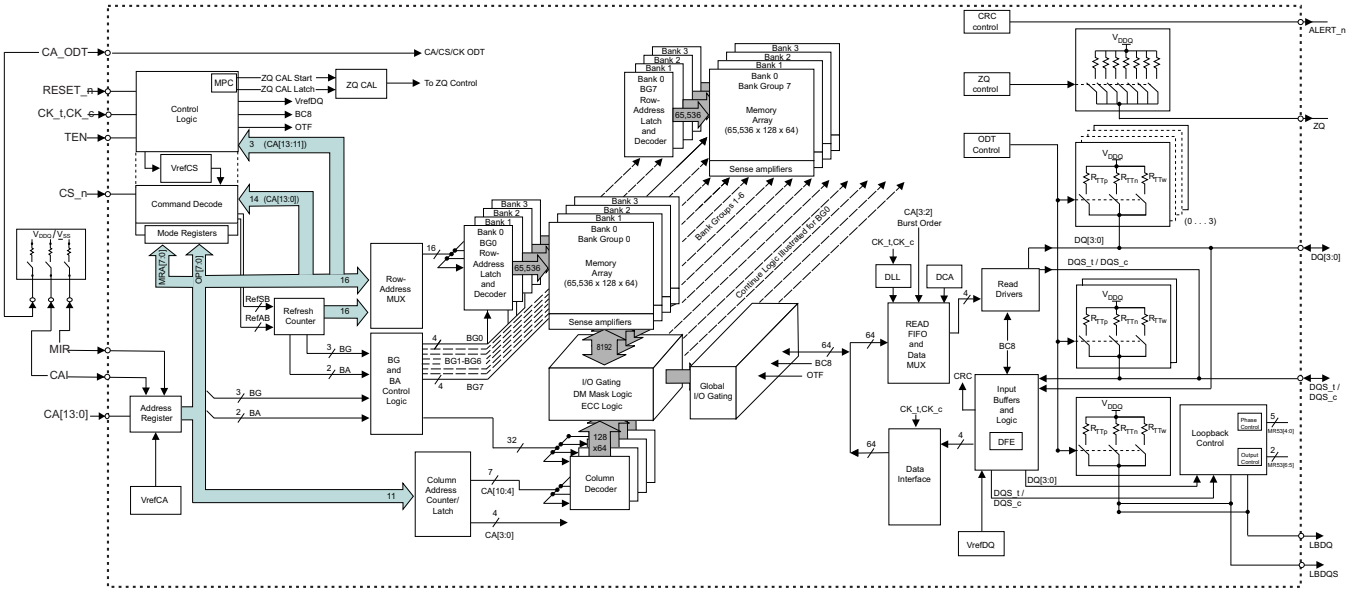


Figure 3: 2 Gig x8 Functional Block Diagram

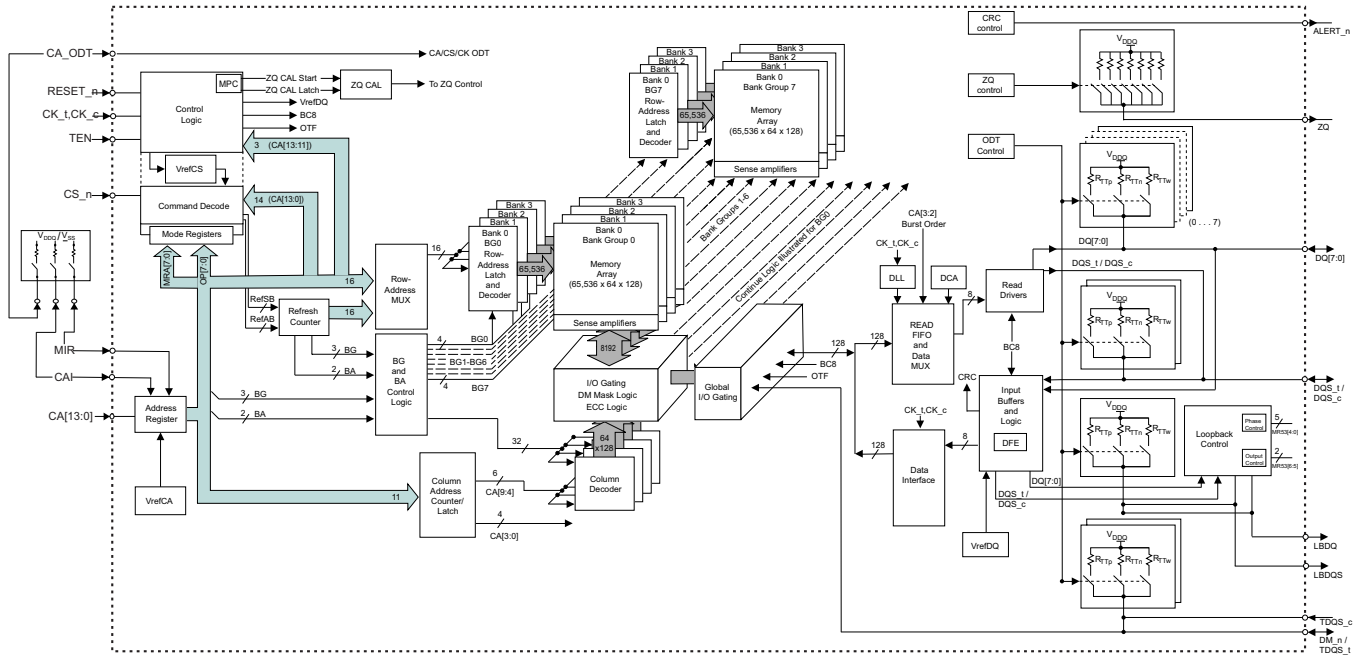
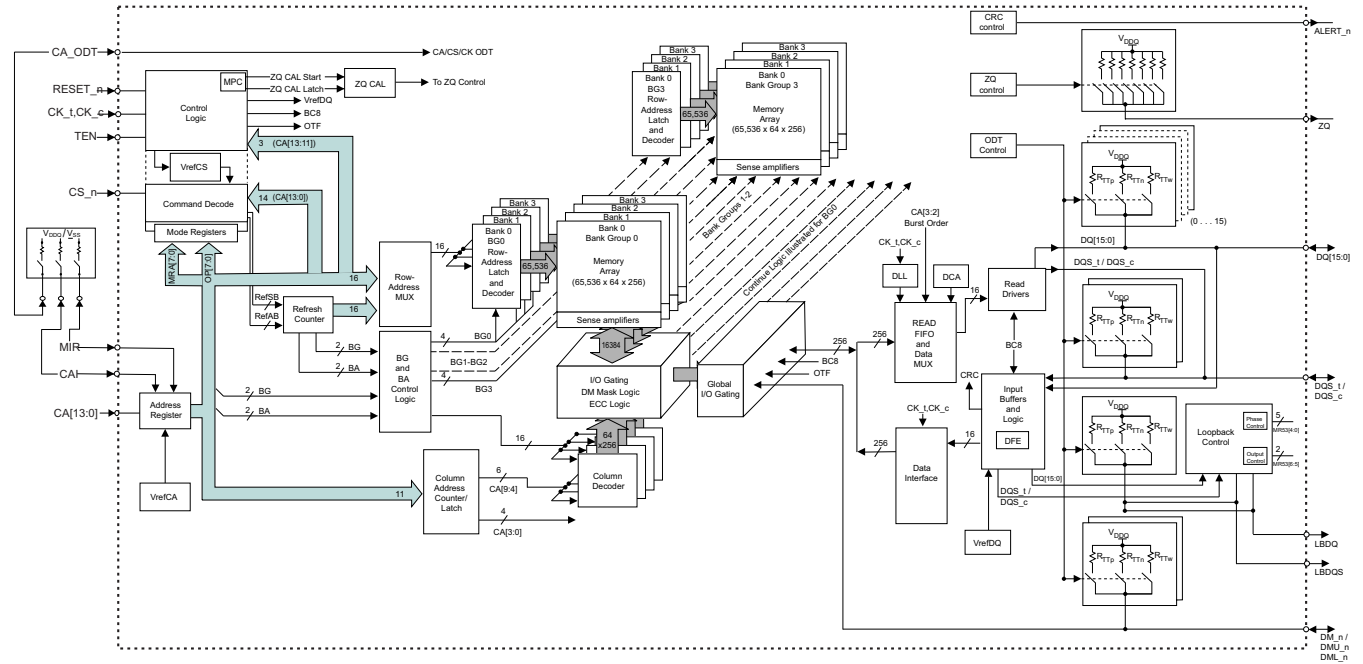


Figure 4: 1 Gig x16 Functional Block Diagram



DDR5 Function Matrix

DDR5 SDRAM has several features supported by configuration width, by density, by speed and by device die Rev. The following table is the summary of the features supported by 16Gb Die Revision D by configuration width. The functional matrix will be defined in each device-specific data sheet; therefore, device, speed and density options will vary by device data sheet.

Table 3: DDR5 Function Matrix - 16Gb Die Rev. D. V: Supported, Blank: Not Supported

Function	x4	x8	x16	MR Default State	Notes
JEDEC Mandatory					
BC8 OTF	V	V	V		
TDQS		V			
Data Mask (DM)		V	V		
Data Output Disable	V	V	V		
Connectivity Test Mode (CT)	V	V	V		
CA/CS/CK ODT	V	V	V		
2N Mode	V	V	V		
Per DRAM Addressability (Enum)	V	V	V		
Mode Register Read (MRR)	V	V	V		
Mode Register Write (MRW)	V	V	V		
Multi-Purpose Command (MPC)	V	V	V		
ZQ calibration	V	V	V		
CA Vref Training	V	V	V		
CS Vref Training	V	V	V		
DQ Vref Training	V	V	V		
CS Training Mode (CSTM)	V	V	V		
CA Training Mode (CATM)	V	V	V		
Write Leveling Training	V	V	V		
DQS Interval Oscillator	V	V	V		
Read Training Pattern Mode (LFSR)	V	V	V		
Write Pattern Command	V	V	V		
Duty Cycle Adjuster (DCA) I	V	V	V	MR42:OP[1:0] = 10(R)	1
Loopback Mode	V	V	V		
Decision Feedback Equalization (DFE)	V	V	V		
WRITE CRC	V	V	V		
READ CRC	V	V	V		
Programmable Preamble	V	V	V		
Programmable Postamble	V	V	V		
sPPR	V	V	V		
hPPR	V	V	V		
PPR using DQ[3:0] only	V	V	V		

Function	x4	x8	x16	MR Default State	Notes
On-Die-ECC	V	V	V		
ECC Transparency and Error Scrub	V	V	V		
Refresh Management (RFM)	V	V	V	MR58:OP[0] = 0 (R)	
				MR58:OP[7:5] = 110 (R)	2
				MR58:OP[4:1] = 1010 (R)	
				MR59:OP[7:6] = 00 (R/W)	
Fine Granularity Refresh (FGR)	V	V	V		
Same Bank Refresh	V	V	V		
Same Bank Precharge	V	V	V		
Maximum power saving mode (MPSM)	V	V	V		
CS Geardown(>= 7200 MT/s)	V	V	V		
JEDEC Optional					
MR65-MR69 Serial Number				MR65 - MR69 = 0x00 (R)	
BL32					
BL32 OTF					
WICA 1/2 step	V	V	V		
Duty Cycle Adjuster (DCA) II	V	V	V	MR42:OP[7] = 1(SR)	
MBIST/mPPR	V	V	V	MR23:OP[4] = 1 (SR)	
sPPR undo/lock	V	V	V	MR23:OP[2] = 1 (SR)	
Adaptive RFM	V	V	V		
Directed RFM	V	V	V	MR59:OP[0] = 1 (SR)	3
				MR59:OP[0] = 0 (W)	
				MR59:OP[2:1] = 00 (R/W)	
				MR59:OP[3] = 0 (R/W)	
Package output driver test mode (PODTM)	V	V	V	MR5:OP[3] = 0 (R)	
Partial array self refresh (PASR)	V	V	V	MR19:OP[7] = 1 (R)	
Refresh interval rate (RIR)	V	V	V	MR4:OP[3] = 1 (SR)	
Rx CTLE (CS_n, CA, DQS)	V	V	V	M22:OP[3] = 1 (R)	
MR4 wide range refresh rate support	V	V	V	MR4:OP[5] = 1 (R)	
Test Mode MR (MR9)					4
ECS Writeback Suppression	V	V	V		
x4 RMW Suppression	V				

Notes: 1. Device supports DCA for four-phase internal clock(s).
2. RAAMMT, RAAIMT, and RAA counter decrement are only applicable if the RFM requirement bit is set to 1 (MR58:OP[0]=1) or ARFM is set to level A, B, or C.
3. Refer to Directed Refresh Management (DRFM) Variance section for specifications regarding this device's variances from the core Design Data Sheet.
4. Test Mode (TM) is a vendor-specific mode register; not used by Micron.

Directed Refresh Management (DRFM) Variance

This section describes this product's support for the DRFM function and its variance from the core design data sheet.

Bounded Refresh Configuration (BRC) and ^{t}DRFM

Use this section's specifications in place of the Bounded Refresh Configuration and ^{t}DRFM subsections under the Refresh Management section of the core design data sheet.

The DRFM command refreshes physically adjacent neighboring rows to the DRFM sampled address, up to the distance specified by the bounded refresh configuration (BRC) as defined by MR59:OP[2:1]. The DRAM is responsible for applying a refresh ratio to rows greater than ±1 to protect the DRAM from excessive refreshes on the outermost rows.

For example, BRC2 will always refresh the ±1 physically adjacent neighboring rows, and the ±2 physically adjacent neighboring rows may be refreshed at a reduced rate as determined by the DRAM. Likewise, if BRC4 is programmed, the device will always refresh the ±1 physically adjacent neighboring rows, while applying a ratio to ±2, ±3, and ±4 physically adjacent neighboring rows.

The corresponding DRFM command duration (^{t}DRFM) is directly related to the time required to refresh the rows. Due to a single row being refreshed on multiple banks corresponding to the DRFMab or DRFMsb command being issued, the per-row-refresh duration is ^{t}RRF, as shown in the table below.

Table 4: ^{t}RRF by Device Density

Parameter	Symbol	8Gb	16Gb	24Gb	32Gb	Units
All bank per row refresh duration	^{t}RRFab (MIN)	70	70	70	70	REF
Same bank per row refresh duration	^{t}RRFsb (MIN)	60	60	60	60	REF

The equation for ^{t}DRFM is (2 * ^{t}RRF) * BRC. ^{t}DRFM is dependent on the DRFMab or DRFMsb command being issued. The table below shows the allowable BRC options and corresponding ^{t}DRFM durations.

Table 5: Bounded Refresh Configuration and ^{t}DRFM Density

MR59:OP[2:1]	Rows Refreshed	^{t}DRFMab	^{t}DRFMsb	Units
BRC 2	Always ±1, Ratio ±2	280	240	ns
BRC 3	Always ±1, Ratio ±2, ±3	420	360	ns
BRC 4	Always ±1, Ratio ±2, ±3, ±4	560	480	ns
RFU	RFU	RFU	RFU	–

BRC Support Level

Use this section's specifications in place of the BRC Support Level subsection under the Refresh Management section of the core design data sheet.

The BRC support level MR59:OP[3] indicates how many BRC options the DRAM can support. MR59:OP[3] is R/W for this device, which supports all BRC options (BRC2, 3, 4) for MR59:OP[3] = 0 or 1.

DDR5 Package Pinout and Assignments

Rows

The x4/x8 device has 13 electrical rows of balls. The x16 device has 17 electrical rows of balls. Electrical is defined as rows that contain signal ball or power/ground balls. Additional rows of inactive balls may be available for mechanical support.

Ball Pitch

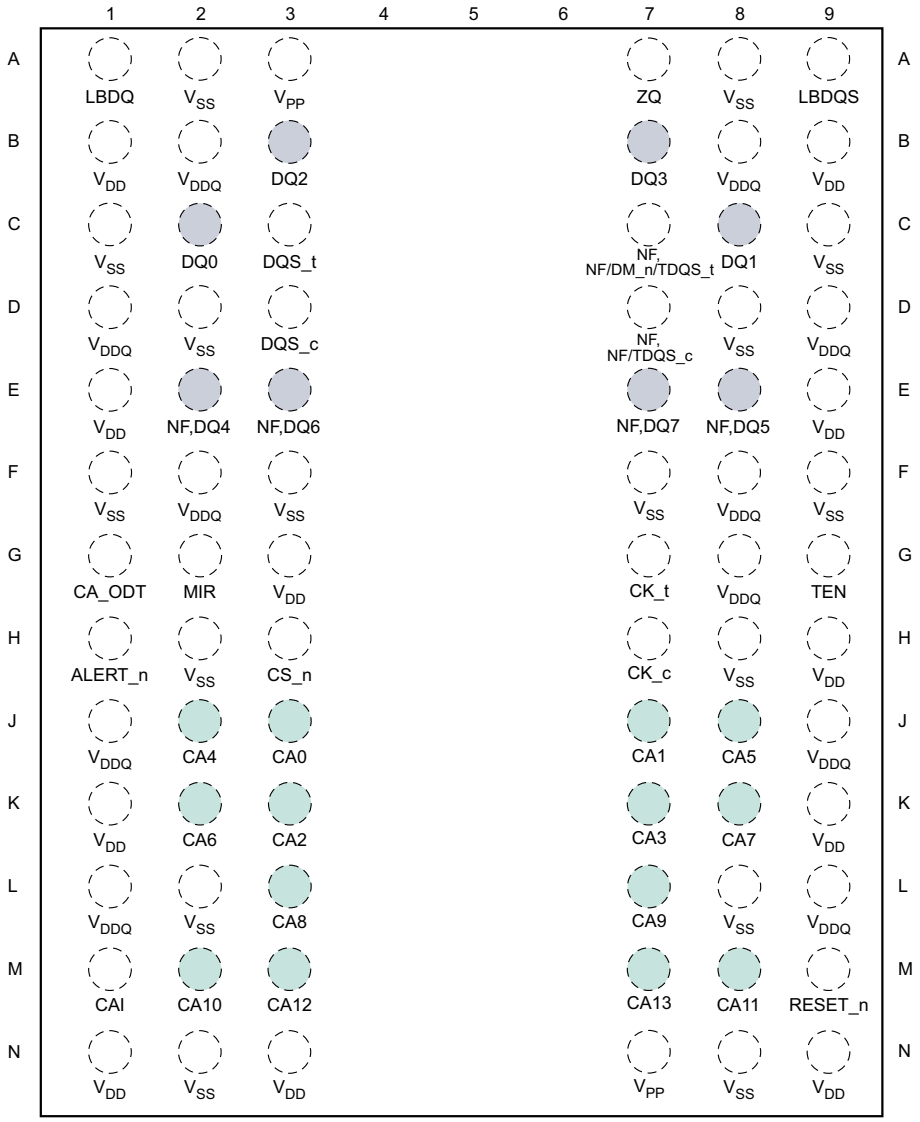
The device uses a ball pitch of 0.8mm x 0.8mm.

Columns

The number of depopulated columns is 3.

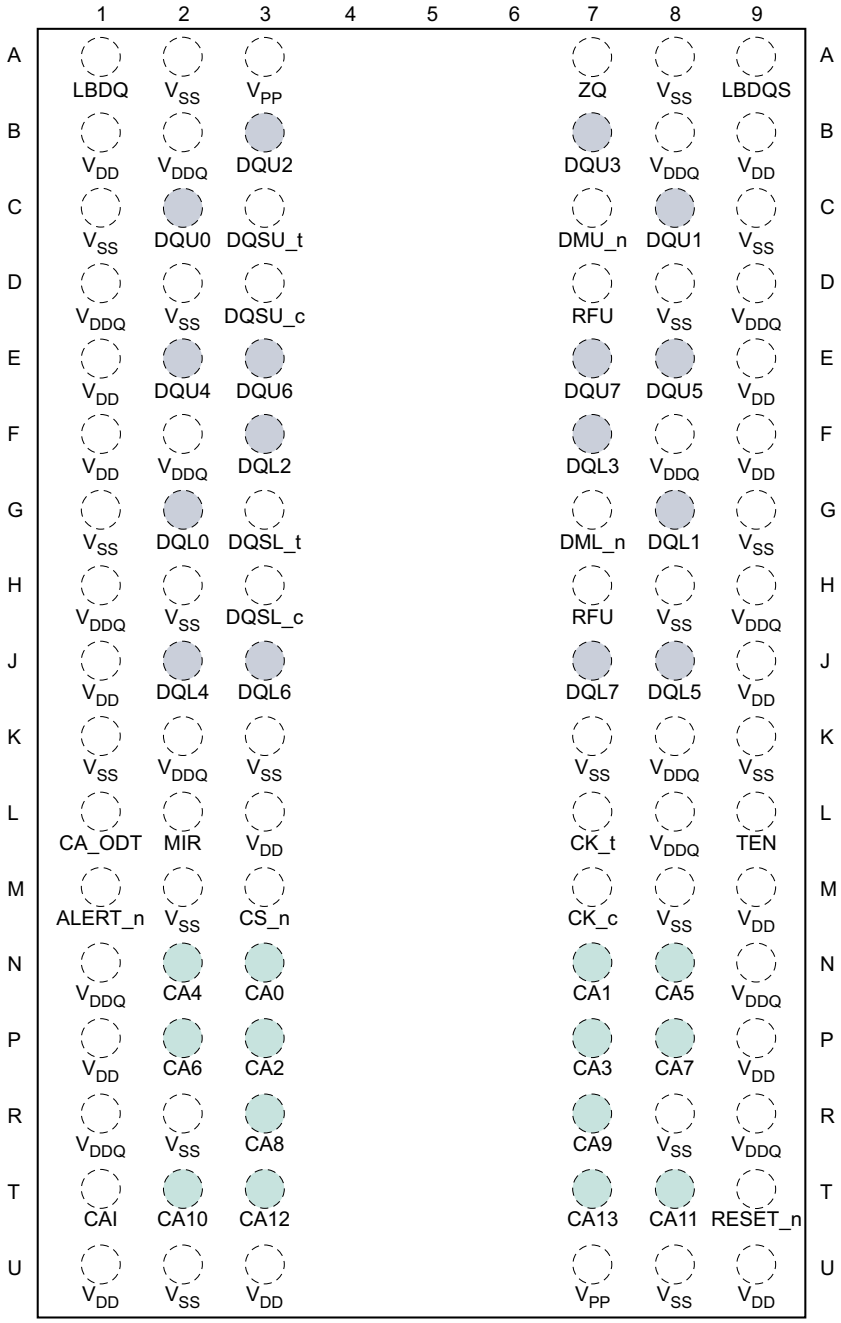
The device has six electrical columns of balls in two sets of three columns. Between the electrical columns are three columns where no balls are populated. Electrical is defined as columns that contain signal ball or power/ground balls. Additional columns of inactive balls may be available for mechanical support.

Figure 5: x4/x8 Ballout Using MO-210-AL – 78-Ball



Notes: 1. Additional columns and rows of inactive balls in MO-210-AL terminal pattern (x4/x8) with support balls are for mechanical support only and should not be tied electrically high or low.
2. Some of the additional support balls can be selectively populated at the suppliers' discretion.
3. DQ4-DQ7 higher-order DQ pins are connected but not used in the x4 configuration.
4. DM, TDQS_t and TDQS_c are not valid for the x4 configuration.
5. A comma "," separates the configuration. A slash "/" defines a mode register-selectable function, command/address function, density or package dependence.

Figure 6: x16 Ballout Using MO-210-AT –102 Ball



Notes: 1. Additional columns and rows of inactive balls in MO-210-AT terminal pattern (x16) with support balls are for mechanical support only and should not be tied electrically high or low.
2. Some of the additional support balls can be selectively populated at the suppliers' discretion.

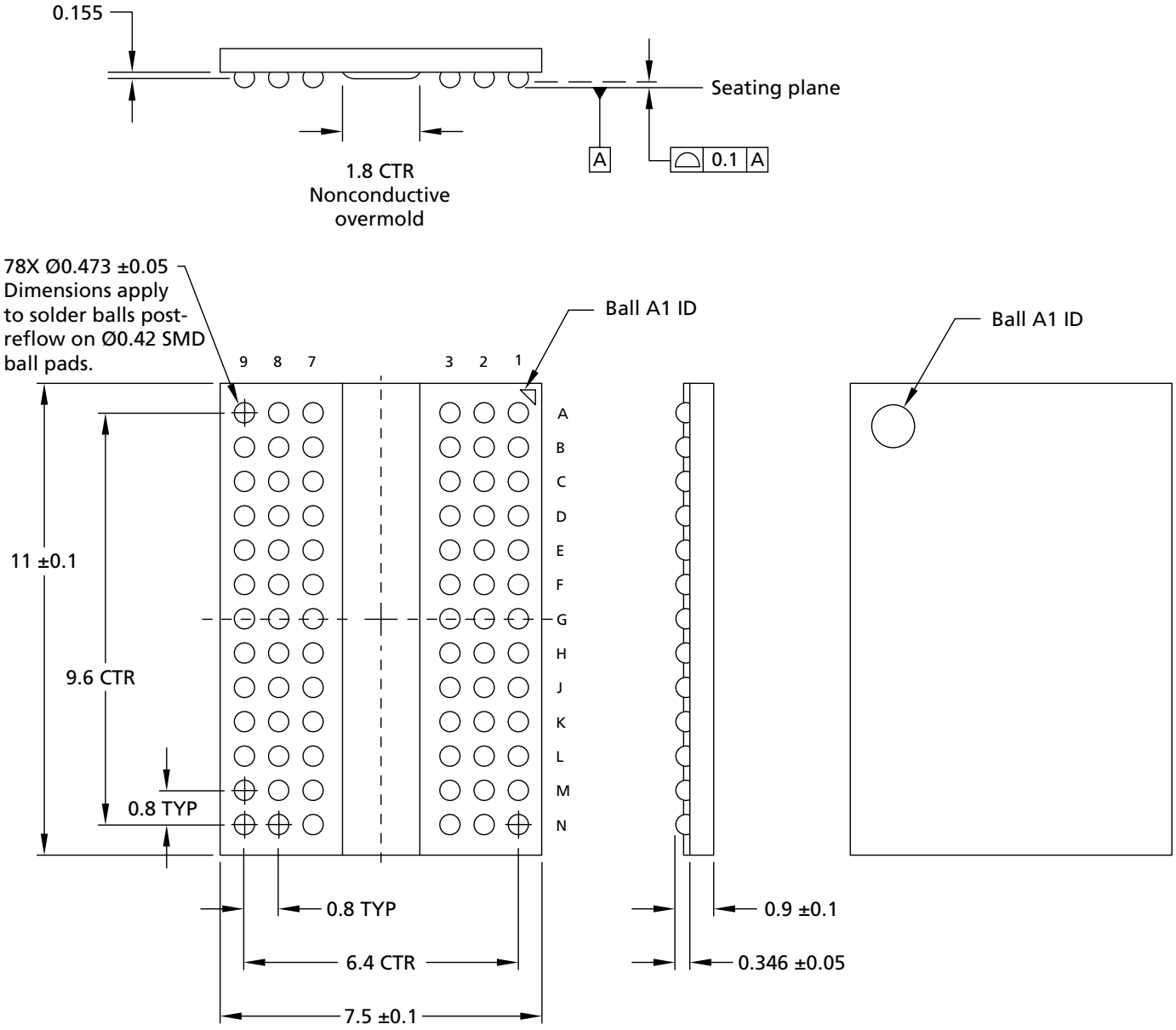
Table 6: Pinout Description

Symbol	Type	Function
CK_t, CK_c	Input	**Clock:** CK_t and CK_c are differential clock inputs. All command/address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CS_n	Input	**Chip Select:** All commands are masked when CS_n is registered HIGH. CS_n provides for external rank selection on systems with multiple ranks. CS_n is considered part of the command code and is used to enter and exit the parts from power down mode and self refresh mode. While not in self refresh mode, the CS_n input buffer operates with the same ODT and V_{REF} parameters as configured by the CA_ODT strap setting or mode register. When in self refresh mode, the CS_n is a CMOS rail-to-rail signal with DC HIGH and LOW at 80% and 20% of V_{DDQ}.
DM_n, DMU_n, DML_n	Input	**Input Data Mask:** DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a write access. DM_n is sampled on both edges of DQS. DM_n is not supported on x4 devices. For x8 devices, the function of DM_n is enabled by the mode register. For x16 devices, the function of DMU_n/DML_n is enabled by the mode register.
CA[13:0]	Input	**Command/Address Inputs:** Command/Address (CA) signals provide the command and address inputs according to the Command Truth Table. Because some commands are multicycle, the pins may not be interchanged between devices on the same bus.
RESET_n	Input	**Active Low Asynchronous Reset:** Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail-to-rail signal with DC HIGH and LOW at 80% and 20% of V_{DDQ}.
DQ	Input/Output	**Data Input/Output:** Bidirectional data bus. If CRC is enabled via the mode register, CRC code is added at the end of a data burst.
DQS_t, DQS_c, DQSU_t, DQSU_c, DQSL_t, DQSL_c	Input/Output	**Data Strobe:** Output with read data, input with write data, edge-aligned with read data, centered in write data. For x16 devices, DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobes DQS_t, DQSL_t and DQSU_t are paired with differential signals DQS_c, DQSL_c, and DQSU_c, respectively, to provide differential pair signaling to the system during reads and writes. The device supports differential data strobe only, not single-ended.
TDQS_t, TDQS_c	Output	**Termination Data Strobe:** Applicable to x8 devices only. When enabled via the mode register, the device enables the same termination resistance function on TDQS_t/TDQS_c that is applied to DQS_t/DQS_c. When disabled via the mode register, DM/TDQS provides the data mask function depending on the MR setting; TDQS_c is not used. x4/x16 devices must disable the TDQS function via the mode register.
ALERT_n	Input/Output	**Alert:** If there is an error in CRC, ALERT_n drives LOW for the period time interval and returns HIGH. During the connectivity test mode, this pin functions as an input. Usage of this signal is system-dependent. In cases where this pin is not connected, ALERT_n must be bonded to V_{DDQ} on the system board.
TEN	Input	**Connectivity Test Mode Enable:** A HIGH on this pin enables CONNECTIVITY TEST MODE operation along with other pins. It is a CMOS rail-to-rail signal with AC HIGH and LOW at 80% and 20% of V_{DDQ}. Usage of this signal is system-dependent. This pin is pulled LOW internally with a weak pulldown resistor to V_{SS} .

Symbol	Type	Function
MIR	Input	**Mirror:** Used to inform the system that this device is being run in mirrored mode instead of standard mode. With the MIR pin connected (strapped) to V_{DDQ}, the device internally swaps even-numbered CA with the next higher odd-number CA. The MIR pin must be tied to V_{SS} if no CA mirror is required. Mirror pair examples: CA2 with CA3 (not CA1) CA4 with CA5 (not CA3). Note: the CA[13] function is only relevant for certain densities (including stacking). In the case that CA[13] is not used, its ball location, considering whether MIR is used or not, should be connected (strapped) to V_{DDQ}. No active signaling requirements required.
CAI	Input	**Command and Address Inversion:** With this pin connected (strapped) to V_{DDQ}, the device internally inverts the logic level present on all CA signals. The CAI pin must be connected to V_{SS} if no CA inversion is required. No active signaling requirements required.
CA_ODT	Input	**ODT for Command and Address:** Apply Group A settings if the pin is connected (strapped) to V_{SS}; apply Group B settings if the pin is connected (strapped) to V_{DDQ}. See the mode register defaults table for details. No active signaling requirements required.
LBDQ	Output	**Loopback Data Output:** The output of this device on the Loopback Output Select defined in MR53:OP[4:0]. When loopback is enabled, it is in driver mode using the default RON described in the Loopback Function section. When loopback is disabled, the pin is either terminated or High-Z based on MR36:OP[2:0].
LBDQS	Output	**Loopback Data Strobe Output:** A single-ended strobe with the rising edged aligned with loopback data edge, falling edge aligned with data center. When loopback is enabled, it is in driver mode using the default RON described in the Loopback function section. When loopback is disabled, the pin is either terminated or High-Z based on MR36:OP[2:0].
RFU	Input/Output	Reserved for future use.
DNU		Do not use.
NF		**No function:** Internal connection is present but has no function.
V_{DDQ}	Supply	DQ power supply; 1.1V nominal.
V_{DD}	Supply	Power supply; 1.1V nominal.
V_{SS}	Supply	Ground
V_{PP}	Supply	Activating power supply; 1.8V nominal.
ZQ	Reference	Reference pin for ZQ calibration. This ball is tied to an external 240 ohm resistor (RZQ), which is tied to V_{SS}.

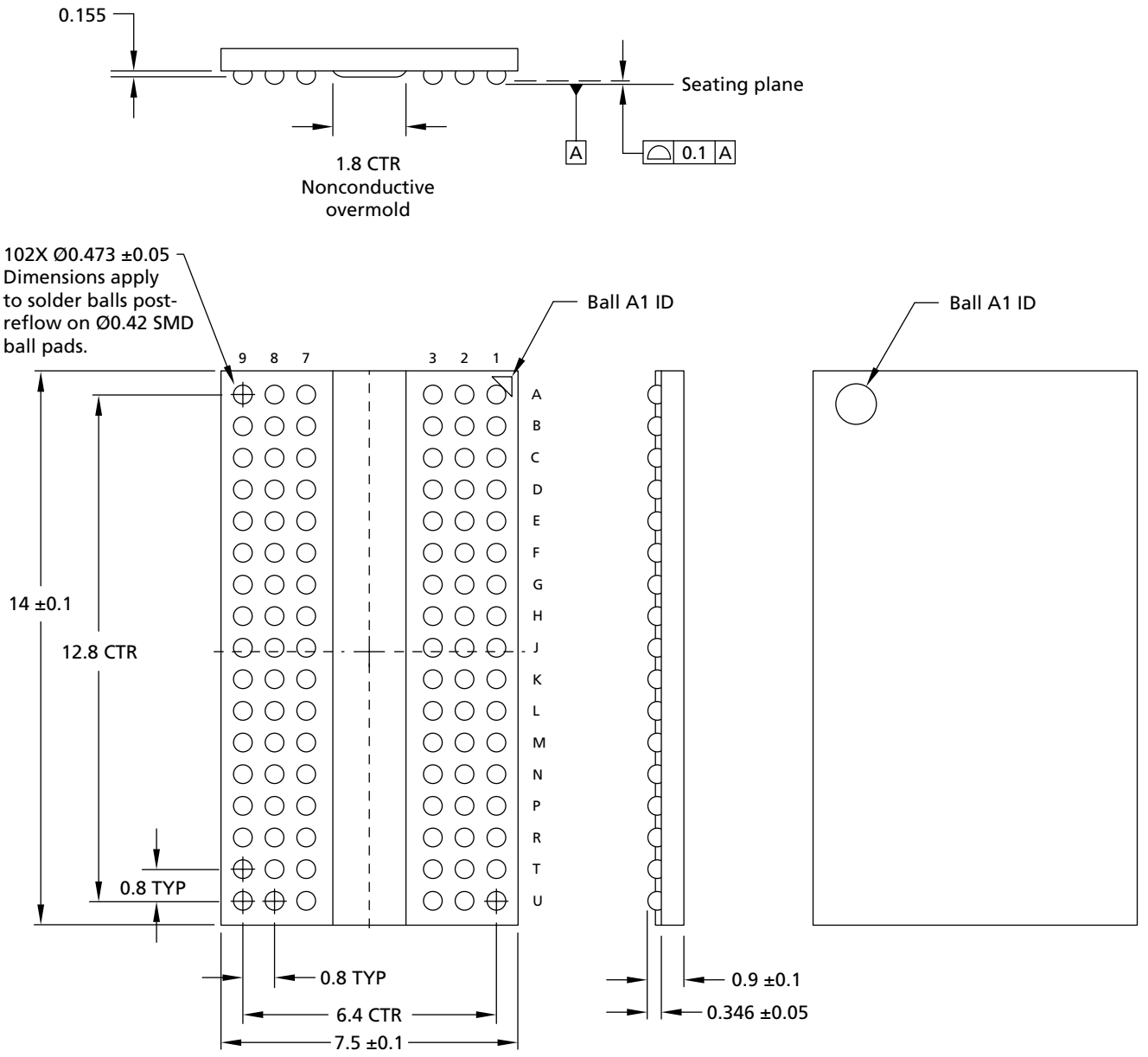
Package Dimensions

Figure 7: 78-Ball VFBGA – MO-210-AL (x4/x8)



Notes: 1. All dimensions are in millimeters.
2. Solder ball material: SACQ (92.45% Sn, 4% Ag, 3% Bi, 0.5% Cu, 0.05% Ni).

Figure 8: 102-Ball VFBGA – MO-210-AT (x16)



Notes: 1. All dimensions are in millimeters.
2. Solder ball material: SACQ (92.45% Sn, 4% Ag, 3% Bi, 0.5% Cu, 0.05% Ni).

Table 7: Package Thermal Resistance Characteristics

Die Revision	Package	Parameter	Value	Unit	Symbol
Rev D	78-ball "RZ"	Junction-to-case (TOP)	4.4	°C/W	ΘJC
		Junction-to-board	16.3	°C/W	ΘJB
	102-ball "HD"	Junction-to-case (TOP)	4.4	°C/W	ΘJC
		Junction-to-board	15.7	°C/W	ΘJB

DDR5 IDD,IPP,IDDQ Current Limits

DDR5 SDRAM current limits are measured and categorized based on the definitions found in the DDR5 Product Core data sheet. Refer to the IDD and IDDQ specification parameters and test conditions for details related to each current limit. Maximum values for I_{DD} currents considering worst-case conditions of process, temperature, and voltage.

Table 8: DDR5 IDD, IPP, IDDQ Current Limits – 16Gb Die Revision D

Parameter	Width	DDR5-5600	DDR5-6400	DDR5-7200	Unit	Notes
IDD0	x4	53	53	TBD	mA	
	x8					
	x16	67	67	TBD		
IPP0	x4	9	9	TBD	mA	
	x8					
	x16	10	10	TBD		
IDDQ0	x4	99	99	TBD	mA	
	x8					
	x16	106	106	TBD		
IDD0F	x4	90	90	TBD	mA	
	x8					
	x16	125	125	TBD		
IPP0F	x4	11	11	TBD	mA	
	x8					
	x16	14	14	TBD		
IDDQ0F	x4	98	98	TBD	mA	
	x8					
	x16	105	105	TBD		
IDD2N	x4	49	49	TBD	mA	
	x8					
	x16					
IPP2N	x4	7	7	TBD	mA	
	x8					
	x16					
IDDQ2N	x4	104	104	TBD	mA	
	x8					
	x16					
IDD2NT	x4	92	98	TBD	mA	
	x8					
	x16					

Parameter	Width	DDR5-5600	DDR5-6400	DDR5-7200	Unit	Notes
IPP2NT	x4	7	7	TBD	mA	
	x8					
	x16					
IDDQ2NT	x4	105	106	TBD	mA	
	x8					
	x16					
IDD2P	x4	47	47	TBD	mA	
	x8					
	x16					
IPP2P	x4	7	7	TBD	mA	
	x8					
	x16					
IDDQ2P	x4	90	90	TBD	mA	
	x8					
	x16					
IDD3N	x4	111	111	TBD	mA	
	x8					
	x16	140	140	TBD		
IPP3N	x4	8	8	TBD	mA	
	x8					
	x16	10	10	TBD		
IDDQ3N	x4	100	100	TBD	mA	
	x8					
	x16	106	106	TBD		
IDD3P	x4	110	110	TBD	mA	
	x8					
	x16	138	138	TBD		
IPP3P	x4	8	8	TBD	mA	
	x8					
	x16	9	9	TBD		
IDDQ3P	x4	84	84	TBD	mA	
	x8					
	x16	93	93	TBD		
IDD4R	x4	226	248	TBD	mA	
	x8	263	286	TBD		
	x16	365	394	TBD		

Parameter	Width	DDR5-5600	DDR5-6400	DDR5-7200	Unit	Notes
IPP4R	x4	9	9	TBD	mA	
	x8	10	10	TBD		
	x16	11	11	TBD		
IDDQ4R	x4	183	252	TBD	mA	
	x8	251	313	TBD		
	x16	462	567	TBD		
IDD4RC	x4	225	246	TBD	mA	
	x8	258	259	TBD		
	x16	357	394	TBD		
IPP4RC	x4	9	9	TBD	mA	
	x8	9	9	TBD		
	x16	11	11	TBD		
IDDQ4RC	x4	195	248	TBD	mA	
	x8	251	280	TBD		
	x16	454	506	TBD		
IDD4W	x4	262	286	TBD	mA	
	x8	269	295	TBD		
	x16	385	429	TBD		
IPP4W	x4	22	22	TBD	mA	
	x8	23	23	TBD		
	x16	38	38	TBD		
IDDQ4W	x4	210	224	TBD	mA	
	x8	303	328	TBD		
	x16	560	610	TBD		
IDD4WC	x4	259	283	TBD	mA	
	x8	266	292	TBD		
	x16	381	425	TBD		
IPP4WC	x4	22	22	TBD	mA	
	x8	23	23	TBD		
	x16	38	38	TBD		
IDDQ4WC	x4	207	221	TBD	mA	
	x8	299	324	TBD		
	x16	554	603	TBD		
IDD5B	x4	432	432	TBD	mA	
	x8					
	x16					

Parameter	Width	DDR5-5600	DDR5-6400	DDR5-7200	Unit	Notes
IPP5B	x4	33	33	TBD	mA	
	x8					
	x16					
IDDQ5B	x4	105	105	TBD	mA	
	x8					
	x16					
IDD5C	x4	148	148	TBD	mA	
	x8					
	x16					
IPP5C	x4	14	14	TBD	mA	
	x8					
	x16					
IDDQ5C	x4	105	105	TBD	mA	
	x8					
	x16					
IDD5F	x4	405	405	TBD	mA	
	x8					
	x16					
IPP5F	x4	31	31	TBD	mA	
	x8					
	x16					
IDDQ5F	x4	105	105	TBD	mA	
	x8					
	x16					
IDD6N(0-85C)	x4	112	112	TBD	mA	1
	x8					
	x16					
IPP6N (0-85C)	x4	15	15	TBD	mA	1
	x8					
	x16					
IDDQ6N (0-85C)	x4	66	66	TBD	mA	1
	x8					
	x16					
IDD6E (85-95C)	x4	186	186	TBD	mA	2
	x8					
	x16					

Parameter	Width	DDR5-5600	DDR5-6400	DDR5-7200	Unit	Notes
IPP6E (85-95C)	x4	20	20	TBD	mA	2
	x8					
	x16					
IDDQ6E (85-95C)	x4	82	82	TBD	mA	2
	x8					
	x16					
IDD7	x4	343	387	TBD	mA	
	x8	386	433	TBD		
	x16	460	516	TBD		
IPP7	x4	24	26	TBD	mA	
	x8	24	26	TBD		
	x16	36	39	TBD		
IDDQ7	x4	244	246	TBD	mA	
	x8	302	309	TBD		
	x16	552	566	TBD		
IDD8	x4	42	42	TBD	mA	
	x8					
	x16					
IPP8	x4	7	7	TBD	mA	
	x8					
	x16					
IDDQ8	x4	92	92	TBD	mA	
	x8					
	x16					

Notes: 1. Applicable for MR4:OP[2:0]=001b, 010b.
2. Applicable for MR4:OP[2:0]=011b, 100b, 101b.

Revision History

Rev. E – 01/2024

- Corrected label for ball C7 in 78-ball, x4/x8 package pinout diagram
- Changed data sheet to Production status

Rev. D – 10/2023

- Added industrial temperature MPNs for x8/x16

Rev. C – 07/2023

- Added IDD Limits for 5600/6400 speeds
- 6400 MPNs moved to Preliminary status

Rev. B – 06/2023

- Updated Package Dimensions to match the 78-Ball VFBGA for x4/x8

Rev. A – 03/2023

- Preliminary Release

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